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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,884	10/24/2003	Alfred I-Tsung Pan	10992304-3	1915

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HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

GUERRERO, MARIA F

ART UNIT PAPER NUMBER

2822

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/692,884

Applicant(s)

PAN, ALFRED I-TSUNG

Examiner

Maria Guerrero

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 14-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This Office Action is in response to the Preliminary Amendment filed October 24, 2003.

### **Status of Claims**

2. Claims 1-13 are canceled. Claims 14-21 are pending.

### ***Specification***

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 14-18 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilson (US 4,890,157).

Wilson teaches adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement

alignment precision (col. 7, lines 34-54). Wilson discloses lithographically processing the unprocessed, integrateable form of a plurality of chips on the upper surface (Abstract, col. 2, lines 35-68, col. 7, lines 34-54). Wilson shows the integrated chips being aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances (col. 7, lines 34-54). Wilson describes the lithographic processing tolerance being  $\pm 1$  micron and the overlay tolerance of  $\pm 1$  mil. (col. 7, lines 34-54). Wilson teaches forming a plurality of alignment holes (slots) and adhering by using alignment pins to mate with corresponding the alignment holes (col. 2, lines 65-68, col. 3, lines 1-10, col. 6, lines 38-68, col. 7, lines 1-12). Wilson discloses using the casting method (curtain coating deposition) as part of the lithographically processing (col. 2, lines 45-47, col. 3, lines 65-68, col. 4, line 1). Wilson teaches the upper surface of the integrated chips being directly formed in parallel, but different plane than the substrate carrier (col. 2, lines 35-4, col. 7, lines 15-50).

In addition, the elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Therefore, the claims are anticipated by Wilson.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US 4,890,157) in view of Leibovitz et al. (5,055,425).

Regarding claim 19, Wilson does not specifically show polishing the upper surface of the plurality of chips. However, Leibovitz et al. discloses using polishing to remove surface irregularities and prepare the surface for the subsequent processing (col. 2, lines 35-38, col. 3, lines 20-30, 53-56, col. 4, lines 34-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Wilson's process by including the step polishing as taught by Leibovitz et al. in order to remove surface irregularities and prepare the surface for the subsequent processing (Leibovitz et al., col. 2, lines 35-38).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Eichhorn et al. (US 5,654,121) is cited as evidence to show casting methods included curtain coating deposition (col. 5, lines 40-41). Jiang et al.


(US 6,428,942), Vafi et al. (US 5,474,458), Jacobs (US 5,055,907), and Beerling et al. (US 6,123,410) show forming a multilayer circuit structure having a plurality of chips.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 9, 2005

  
**MARIA F. GUERRERO**  
**PRIMARY EXAMINER**